CIRCUIT AND METHOD FOR IMPROVED BACK ELECTROMOTIVE FORCE DETECTION

Priority

[1] This application is a continuation-in-part of and claims priority from United States patent application entitled CIRCUIT FOR IMPROVED BACK EMF DETECTION filed on November 20, 2001, under serial number 09/991,325, which application is incorporated by reference for all purposes.

TECHNICAL FIELD

[2] The present invention relates generally to motor driving and control circuitry, and is more specifically related to an improved circuit and method for back electromotive force (back EMF) detection in a brushless motor.

DISCUSSION OF RELATED ART

[3] Three-phase brushless DC motors have many uses, among which include both high-speed and low -speed applications. Conventional high-speed applications include spindle motors for computer hard disk drivers, digital video disk (DVD) drivers, CD players, tape-drives for video recorders, and blowers for vacuum cleaners. A motor for high-speed applications typically operates in a range from a few thousand rotations per minute (rpm's) to 20,000 rpm' s, for example. Conventional low-speed applications include motors for farm and construction equipment, HVAC compressors, and fuel pumps. Motors for low-speed applications typically operate in a range from less than a few hundred rpm's to a few thousand rpm's, for example. Compared to DC motors employing brushes, brushless DC motors enjoy reduced noise generation and improved reliability because no brushes need to be replaced due to wear.

[4] **FIG. 1** is a cross-section of a typical conventional brushless DC motor ***10***. The motor ***10*** includes a permanent magnet rotor ***12*** and a stator ***14*** having a number of windings (***A***, ***B***, ***C*** shown in **FIG. 2**). The windings are each formed in a plurality of slots ***18***. Although the rotor ***12*** is shown housed within the stator ***14***, the stator ***14*** may also be housed within the rotor ***12***. The rotor ***12*** is permanently magnetized, and turns to align its own magnetic flux with the flux generated by the windings.

[5] Power to the motor ***10*** is often provided in a pulse width modulation (PWM) mode. The PWM mode is a nonlinear mode of power supply in which the power is switched on and off at a very high frequency in comparison to the angular velocity of the rotor. For example, typical switching frequencies may be in the range of 20 kHz. In a typical on-off cycle lasting about 50 μS, there may be 40 μS of "on" time followed by 10 μS of "off' time. Given the short duration of off times, current still flows through the motor windings so there is virtually no measurable slow down in the angular velocity of the rotor ***12*** during these periods. Accordingly, PWM mode provides a significant power savings advantage over modes in which power is continuously supplied.

[6] In order to operate the motor ***10***, the flux existing in the stator ***14*** is controlled to be slightly in advance of the rotor ***12,*** thereby continually pulling the rotor forward. Alternatively, the flux in the stator ***14*** may be controlled to be just behind the rotor ***12***, in which case the polarity is set such as to continually repel the rotor ***12*** forward. Therefore, to optimize the efficiency of the motor ***10***, it is advantageous to monitor the position of the rotor ***12*** so that the flux in the stator ***14*** may be appropriately controlled and switched from one commutation stage to the next in the commutation sequence. If the rotor ***12*** movement and the flux rotation should ever get out of synchronization, the rotor ***12*** may become less efficient, start to jitter, or stop turning.

[7] A conventional motor can be represented in circuit form as having three coils ***A***, ***B***, and ***C*** connected in a "Wye" or "Y" configuration, as shown by reference numeral ***20*** in **FIG. 2**, although a larger number of stator coils are often employed with multiple rotor poles. Typically, in such applications, eight-pole motors are used having twelve stator windings and four N-S magnetic sets on the rotor, resulting in four electrical cycles per revolution of the rotor. The stator coils, however, can be analyzed in terms of three "Y" connected coils, connected in four sets of three coils, each physically separated by 90 degrees.

[8] In operation, coils ***A***, ***B*** and ***C*** are energized with a PWM drive signal that causes the coils to generate magnetic fields. The resulting attraction/repulsion between the magnetic fields of the coils ***A***, ***B***, and ***C*** and the magnetic fields created by the magnets in the motor causes the rotor ***12*** to rotate.

[9] The coils are energized in sequences to produce a current path through two coils of the "Y", with the third coil left floating (or in tri-state), hereinafter floating coil FC. The sequences are arranged so that as the current paths are changed, or commutated, one of the coils of the current path is switched to float, and the previously floating coil is switched into the current path. The sequences are defined such that when the floating coil is switched into the current path, the direction of the current in the coil that was included in the prior current path is not changed. In this manner, six commutation, sequences, or phases, are defined for each electrical cycle in a three phase-motor, as shown in Table A.

Table A

Phase	Current Flows From:	Current Flows To:	Floating Coil
1	A	B	C
2	A	C	B
3	B	C	A
4	B	A	C
5	C	A	B
6	C	B	A

[10] When the motor is turning, rotation of the rotor induces a back electromotive force EMF voltage ***e*** in each of the coils or windings of the motor. Such back EMF is represented by the Bemf voltage sources in **FIG. 2**. With respect to whichever phase is currently floating, the back EMF voltage ***e*** in that phase is monitored to determine when to advance in the communication sequence. More particularly, the back EMF voltage ***e*** in the floating coil is monitored to determine when it crosses zero, at which point the position of the rotor is assumed to be known. The point at which the back EMF voltage ***e*** crosses zero is referred to as the "zero crossing." Each time a zero crossing is detected, the motor advances in its commutation sequence by 30 electrical degrees (by one phase of Table A).

[11] A conventional technique to measure the back EMF voltage ***e*** is to measure, during a floating period, the voltage at a coil tap ***Va***, ***Vb***, and ***Vc***, for the floating coil. The measured voltage at the coil tap is presumed to be the back EMF voltage ***e***. Accordingly, the coil-tap voltage for the floating coil is monitored to detect zero crossings at which times the commutation sequence is advanced.

However, unless the center tap voltage V_{CT} is zero, this back EMF measurement is not fully accurate.

[12] Known methods of detecting back EMF voltage ***e*** include comparing the floating-phase coil-tap voltage with the center tap voltage, or a virtual center tap voltage configured by a resistor network. During the PWM-on and PWM-off states, the center tap voltage V_{CT} is significantly deviated from zero. This generates high common-mode noise. To offset the center tap voltage V_{CT} for zero-crossing detection, voltage divider and filter circuits have been used. However, such voltage divider and filter circuits reduce the sensitivity of the circuits and delay zero-crossing detection.

SUMMARY OF THE INVENTION

[13] In one embodiment of the invention, a circuit and a method provide a back EMF signal that represents a back EMF voltage induced in a coil of a brushless motor. The circuit includes an input node operable to receive a tap voltage from the coil, and a network coupled to the input node and operable to generate the back EMF signal by removing a predetermined offset voltage from the tap voltage. Such a circuit provides a signal that more accurately indicates a zero crossing than existing circuits for controlling a sensorless brushless motor.

BRIEF DESCRIPTION OF THE DRAWINGS

[14] **FIG. 1** shows a cross section of a known brushless, permanent magnet motor;

[15] **FIG. 2** shows a schematic diagram of a known circuit for controlling the motor of **FIG. 1**;

[16] **FIG. 3** is a theoretical timing diagram depicting the voltages and zero crossings detected in each of three phases of the circuit shown in **FIG. 2** with the PWM signal removed;

[17] **FIG. 4** illustrates a driver circuit for a brushless DC motor according to an embodiment of the present invention;

[18] **FIG. 5** is a schematic diagram of a precondition circuit for phase A of the motor illustrated in **FIG. 4**, according to an embodiment of the present invention;

[19] **FIG. 6** is a schematic timing of a precondition circuit and the zero-crossing detector ***52*** arranged for compensating the induced signals ***Va***, ***Vb***, and ***Vc*** from the three phases of the motor illustrated in **FIG. 4**, according to an embodiment of the present invention; and

[20] **FIG. 7** is a theoretical graph illustrating the compensated signals ***Ea***, ***Eb***, ***Ec*** of precondition circuit of **FIG. 6**, and resulting output from the zero-crossing detection circuit, according to an embodiment of the invention

DETAILED DESCRIPTION

[21] Embodiments of the present invention will now be described with reference to the drawings, wherein like reference labels are used to refer to like elements throughout.

[22] Referring initially to **FIG. 2**, there is shown an electrical schematic diagram of a conventional motor ***20*** having three coils ***A***, ***B***, and ***C*** connected in a "Y" configuration. As will be described in more detail below, embodiments of the present invention provide an improved method and apparatus for advancing the commutation sequences of the motor ***20*** by monitoring for zero crossings during PWM-off states. During such PWM-off states, a precondition circuit ***50***, (**FIG. 4**) is used to offset variances in back EMF voltage ***e*** as measured at a coil tap, which occur due to a non-zero center tap voltage V_{CT}. While the precondition circuit ***50*** is useful in any brushless DC motor application, it finds particular benefit in low-speed and/or low-voltage motor applications as discussed in more detail below.

[23] The motor ***20*** comprises three phases or coils ***A***, ***B***. ***C***. Each phase has a respective inductor ***La***, ***Lb***, ***Lc*** and line resistance ***Ra***, ***Rb***, ***Rc***. The three phases may be connected in a star ("Y") configuration having a center tap ***CT***, or in a delta configuration (not shown). Embodiments of the invention may be applied to either. For each coil, a pair of switches ***Xsa***, ***Xga***, ***Xsb***, ***Xgb***, ***Xsc***, ***Xbc*** (collectively "switch(s) ***X***") connect a free end of a coil (also referred to as a coil tap) at ***Va***, ***Vb***, ***Vc***, to supply ***Vs*** and GND voltages, respectively. The switches are

typically power transistors such as Mosfets or the like. A reverse biased diode ***Dsa***, ***Dga***, ***Dsb***, ***Dgb***, ***Dsc***, ***Dgc*** (collectively "diode(s) ***D***") is placed in parallel with (or may be inherently within) each of these switches. The diodes are power rectifiers, and typically serve to protect the switches and windings against induced voltages exceeding the supply or ground voltage. As described in more detail below, during PWM-off states, the voltage drop across the diodes ***D*** has been found to cause the center tap voltage V_{CT} to deviate from zero which, in turn, creates undesirable variances in measurement of the back EMF voltage ***e***.

[24] Continuing to refer to **FIG. 2**, it will be described below, by way of example, how the diodes ***D*** deviate the center tap voltage ***CT*** from zero during a PWM-off state. For this example, it is presumed that the motor ***20*** is in its first phase of a six-phase commutation sequences, wherein current flows from phase A to phase B, while phase C is left floating. Further, it is presumed preferably that during the PWM-off state, the PWM signal does not turn on the switch ***Xga*** coupling phase A to ground. In this manner, during the PWM-off state, all of the current freewheeling from phase A to phase B passes through diode ***Dga***. By not turning on, during the PWM-off state, the switch that couples the high phase (*e.g.* the phase "from" which current is flowing in a given commutation phase) to ground, there is reduced switching loss and noise introduced into the motor ***20***. It will be appreciated, however, that the present invention may be applied to motors which turn on the switch (*e.g.* ***Xga***) coupling the high phase to ground during PWM-off periods, except that in such circumstances the precondition circuit ***50*** is appropriately adjusted to take into account the fact that all of the current during the freewheeling period is not passing through the diode (*e.g.* ***Dga***) alone.

[25] In view of the above assumptions, and by way of example, the following equations can be derived from **FIG. 2**:

[26] If phases A and B are conducting current, phase C is floating and the terminal voltage ***Vc*** may be detected. When the up transistor ***Xga*** is turned off, the current freewheels through the diode ***Dga***. During this freewheeling period, and because there is no current in phase C, coil (or winding) ***Lc*** induces a phase C back EMF voltage e_c measurable at coil tap ***Vc*** along with any other voltages present in phase C.

[27] When summing the voltages around phase C; $v_c = e_c + v_n$. The induced signal v_c at coil tap ***Vc*** equals the back EMF signal $_c$ only when v_n equals zero (or V_{CT} as shown in **FIG. 2**). In fact, v_n is typically not zero because of an offset or distortion introduced by components of the motor driver.

For phase A, we have

$$v_n = 0 - v_d - ri - L\frac{di}{dt} - e_a \qquad (1)$$

For phase B, we have

$$v_n = v_{mos} + ri + L\frac{di}{dt} - e_b \qquad (2)$$

Where v_d is the forward voltage drop of the diode ***Dga***, v_{mos} is the voltage drop on MOSFET ***Xgb***, v_n is the center tap voltage (***Vct*** of **FIG. 2**), $_r$ is the resistor ***R*** of the phase, L is the coil or winding inductance of the phase, and ***e*** is the induced back EMF voltage (***Bemf*** in **FIG. 2**) of the phase.

Adding equations (1) and (2), we get

$$2v_n = v_{mos} - v_d - (e_a + e_b) \qquad (3), \text{ and}$$

$$v_n = \frac{v_{mos} - v_d}{2} - \frac{e_a + e_b}{2} \qquad (4)$$

Also from the balanced three-phase system, we have

$$e_a + e_b + e_c = 0 \qquad (5)$$

From (3) and (4),

$$v_n = \frac{v_{mos} - v_d}{2} + \frac{e_c}{2} \qquad (6)$$

So, the terminal voltage Vc,

$$v_c = e_c + v_n = \frac{3}{2}e_c + \frac{v_{mos} - v_d}{2} \qquad (7)$$

If we ignore the second term of (7), the induced signal $\boldsymbol{v_c}$ at coil tap ***Vc*** is a function of the back EMF voltage $\boldsymbol{e_c}$. However, especially at low speed and low voltage, the back EMF voltage $\boldsymbol{e_c}$ is very small. Accordingly, one-half of the diode voltage of approximately 0.5 volts will significantly affect the induced signal $\boldsymbol{v_c}$ for a system driving a 12-volt motor. Thus, the second term of equation (7) plays a significant role.

For a low voltage MOSFET, Rd is very low and its Vmos can be ignored, so (7) can be rewritten as,

$$v_c = e_c + v_n = \frac{3}{2} e_c - \frac{v_d}{2} \qquad (8)$$

[28] The above equations demonstrate that the induced signal v_c at the coil tap ***Vc*** is proportional to the back EMF e_c of Phase C with the exception of one-half of the voltage across the diode ***Dga***, shown as voltage ***Vd*** in equation (8). As described below, an embodiment of the claimed invention provides a precondition circuit for compensating or offsetting the effect of diode ***Dga***, or compensating for any other distortion in the induced signal v_c at coil tap ***Vc***.

[29] **FIG. 3** is a theoretical timing representation of the zero-crossing detection in a motor ***20*** that does not include the precondition circuitry ***50***. The graph of **FIG. 3** shows theoretical data presuming, for sake of simplicity, the high-frequency PWM signal has been removed. Ideally, zero crossings of each phase A, B, C of the motor ***20*** would be distributed evenly in 60-degree intervals. However, the detection of the zero crossing for each phase is unsymmetrical due to the effect of the diodes ***D*** during the PWM-off states. More particularly, as shown in **FIG. 3**, each time the coil-tap voltage ***Va***, ***Vb***, ***Vc*** crosses zero, a zero-crossing signal ***30*** is shown to transition from high-to-low or low-to-high. Due to the effect of the diodes ***D*** as indicated by equation (8) above, the zero-crossing signal ***30*** does not transition in equal 60-degree intervals.

[30] Referring briefly back to **FIG 2**, in systems not having the precondition circuitry ***50***, the zero-crossing signal ***30*** was typically obtained by comparing the floating-phase coil-tap voltage, such as voltage ***Vc***, with a reference voltage ***Rref*** by way of a comparator ***35***. While for sake of example only phase ***C*** is shown to be coupled to a comparator ***35*** for detecting zero crossings, it will be appreciated that each phase ***A***, ***B***, and ***C*** is coupled to a comparator for this purpose. In especially low-voltage and/or low-frequency applications, it has been determined that because the slope of change of the coil-tap voltage ***Va***, ***Vb***, and ***Vc*** as it approaches zero crossing is very gradual, accurately detecting the time a zero-crossing actually occurs can be difficult. In particular, with a gradual change in coil-tap voltage around zero crossing, the actual timing of the zero crossing is

often difficult to determine in view of the inherent standard deviation/offset of the comparator ***35***.

[31] **FIG. 4** illustrates a driver circuit for a brushless DC motor ***100***, according to an embodiment of the present invention. The motor ***100*** is substantially similar to the motor ***20*** described above with reference **FIG. 2** and, therefore, common elements will not again be discussed. However, in addition to the elements described above, the motor ***100*** of the present invention includes a precondition circuit ***50*** that includes networks ***50a, 50b,*** and ***50c***, coupled respectively to the coil taps ***Va***, ***Vb***, and ***Vc*** for each phase. As described in detail below, the precondition circuit ***50*** includes circuitry for offsetting or compensating the coil-tap voltage ***Va***, ***Vb***, and ***Vc*** from the effect of the diodes ***D***. An output of the precondition circuit ***50*** is coupled to a zero-crossing detection circuit ***52***. The zero-crossing detection circuit ***52*** may, for example, take the form of the comparator ***35*** described above with reference to **FIG. 2** or other known circuits known in the art for detecting zero crossings.

[32] **FIG. 5** is a schematic diagram of a network ***50a*** for phase ***A*** illustrated in **FIG. 4**, according to an embodiment of the present invention. However, it will be appreciated that similar networks ***50b*** and ***50c*** are coupled to phases ***B*** and ***C*** as shown in **FIG. 4**. The networks ***50a-c*** of the present embodiment includes circuitry for offsetting the voltage offset of the diode ***D*** from the induced signal ***v*** , so that the outputted back EMF signal ***Ea*** is substantially directly proportional to the back EMF voltage ***e***. As used herein, "back EMF signal" means a signal related to the back EMF voltage ***e***, particularly with respect to the zero crossing feature. For example, as shown in equation (9) below, the "back EMF signal" ***Ea*** may be 3/2 of the back EMF voltage ***e***.

[33] The network ***50a*** includes a node ***Nva*** for receiving an induced signal ***Va***, a node ***Nea*** for outputting the back EMF signal ***Ea***, a control voltage ***Vcon***, and resistors ***R1***, ***R2***, and ***R3***. Resistor ***R1*** is coupled between the node ***Nva*** and a node ***Na'***, the resistor ***R2*** is coupled between the control voltage ***Vcon*** and the node ***Na'***, and the resistor ***R3*** is coupled between the node ***Na'*** and the node ***NEa***. The voltage ***Vcon*** and the resistors ***R1*** and ***R2*** are selected to compensate for the

offset voltage ***Vd/2*** that is introduced into the induced signal ***Va*** by the diode ***D*** such that Vcon x R1/(R1+R2)=Vd/2.

Specifically, for phase ***A***:

$$Ea = Va' = Va + Vcon * R1/(R1 + R2) \quad (9)$$

Also from equation (8)

$$Va = \frac{3}{2} e_a - \frac{v_d}{2} \quad (10)$$

If we select Vcon, R1, and R2 such that

$$Vcon * \frac{R1}{R1 + R2} = \frac{Vd}{2} \quad (11)$$

Then, combining equations (9) and (10) results in

$$Va = \frac{3}{2} e_a - \frac{v_d}{2} + \frac{v_d}{2} = \frac{3}{2} e_a \quad (12)$$

As demonstrated by the above equations, the back EMF signal ***Ea*** is directly proportional to the back EMF voltage e_a when negligible current flows through ***R3***, which is a current limiting resistor. In a driver controlling a 12-volt motor, typical values may be 1k ohms for ***R1***, 10k ohms for ***R2***, 4.7k ohms for ***R3***, and 5 volts for ***Vcon***.

[34] **FIG. 6** is a schematic diagram of the precondition circuit ***50*** including networks ***50a-c***, and the zero-crossing detector ***52***, arranged for compensating the induced signals ***Va***, ***Vb***, and ***Vc*** for the three phases ***A***, ***B***, and ***C*** of the motor ***100*** of **FIG. 4**, according to an embodiment of the present invention. The precondition circuit ***50*** is an extension of the network ***50a*** of **FIG. 5**, where three resistive networks are provided to compensate the three induced voltages ***Va***, ***Vb***, and ***Vc***. Alternatively, each network may receive a different voltage ***Vcon***, and/or include different resistor values. In one embodiment, R1=R4=R7, R2=R5=R8, and R3=R6=R9.

[35] Continuing to refer to **FIGS. 4 and 5**, and using phase ***A*** as an example, in order to offset the effect from the diode ***Dga*** on the signal ***Va*** at the coil tap ***Va***, the network ***50a*** includes a voltage-divider circuit. Node ***Nva*** is coupled to the coil tap ***Va*** to receive the induced voltage ***Va***. Node ***NEa*** is coupled to an input of the zero-crossing detector ***52***. The resistive network of ***R1*** and ***R2***,

and ***Vcon*** offsets the induced voltage ***Va*** of the phase ***A*** coil tap ***Va*** by Vd/2, providing the induced signal ***Va'*** at node ***Na'*** and signal ***Ea*** at node ***NEa*** that are directly proportional to the back EMF voltage ***e*** of phase ***A***. In this manner, the network ***50a*** is able to add a constant voltage to the induced signal ***Va*** that substantially eliminates the effect of the diode ***D***.

[36] It will be appreciated that while values for ***Vcon***, ***R1*** and ***R2*** are stated above for sake of example, other values could have been chosen to achieve a similar result. Further, it will be appreciated that while the networks ***50a-c*** are shown to be formed of a voltage-divide circuit, the present invention is intended to cover any circuit configuration active or passive which serves to offset the value of the diode ***D*** or any other distortion, and is not limited to a voltage-divide circuit. Additionally, as mentioned above, in the present example during a PWM-off state, the switch ***Xga*** in the high phase is not turned on in order to minimize switching loss and noise. Thus, in the example leading to equation (9) the effect of the diode ***Dga*** was shown to be VDga/2. It will be appreciated, however, that the present invention is suitable for use in other motor configurations where, for example, the ground switch (*e.g.* ***Xga***) for the high phase is turned on during a PWM-off state. In such cases, the effect of the diode ***D*** on the coil-tap voltage will differ from the VDga/2 described in the above example. Accordingly, in such alternative embodiments, components of the precondition circuit ***50*** are correspondingly adjusted to offset the effect of the "on" ground switch ***Xga*** by an appropriate amount as can be readily determined by one in the art.

[37] The operation of the precondition circuit ***50*** and the networks ***50a-c*** are now described with reference to **FIGS. 4-6** according to an embodiment of the invention. The motor ***100*** is driven by a PWM signal ***110*** that is applied to the motor ***100*** in one of several conventional manners. For example, in one embodiment, during PWM-on states, the high switch (*e.g.* ***Xsa***, ***Xsb***, ***Xsc***) for the "from" phase of the commutation sequence and the ground switch (*e.g.* ***Xga***, ***Xgb***, ***Xgc***) for the "to" phase of the commutation sequence are turned on. During the following PWM-off state, the high switch in the "from" phase is turned off and all of the freewheeling current is allowed to pass through the diode (*e.g.* ***Dga***, ***Dgb***,

Dgc) in the "from" phase to ground through the ground switch in the "to" phase. Such a current path during the PWM-off state is representatively depicted in **FIG. 4** by current path i_{off}. By not turning on the ground switch in the "from" phase during the PWM-off state, it is possible to avoid switching delays and noise. However, it will be appreciated that the present invention is suitable for motors ***l00*** that operate in any switching mode.

[38] The motor ***l00*** advantageously monitors for zero-crossing detections during PWM-off states. Because a PWM signal typically oscillates at a frequency significantly greater than the frequency at which the commutation sequence advances, zero crossings which may happen to occur during a PWM-on state are still detectable during the PWM-off state with minimal delay. For example, the frequency of the PWM signal may be in the range of 20 kHz-l00 kHz while the frequency at which the commutation sequence advances is typically on the order of 100 Hz. Further, by performing zero-crossing detection during PWM-off states, filters and delays associated with offsetting the center tap voltage ***CT*** during PWM-on states are avoided.

[39] During PWM-off states, zero-crossing detection occurs by providing the induced signal from coil taps ***Va***, ***Vb***, and ***Vc*** for the floating phase to nodes ***Nva***, ***Nvb***, and ***Nvc***, respectively, of the precondition circuit ***50***. The networks ***50a-c*** of precondition circuit ***50*** then offset the induced signal for the effect of the diode ***D*** and the resulting signals ***Ea***, ***Eb***, ***Ec*** are proportional to the back EMF voltage ***e*** for each phase. For instance, in the present example, the precondition circuit ***50*** adjusts the induced signal at the floating phase coil taps ***Va***, ***Vb***, and ***Vc*** by an amount substantially equal to an amount by which the voltage at the center tap ***Vn*** (also shown as V_{CT}) is deviated from zero as discussed above with reference to equations (6) & (7).

[40] Following the offset of the precondition circuit ***50***, the output of the precondition circuit is provided to the zero-crossing detection circuit ***52***. The zero-crossing detection circuit ***52*** may, for example, include a comparator for comparing the output of the precondition circuitry with a reference voltage to determine when a zero crossing has occurred. As the precondition circuit ***50*** of the present invention has adjusted the induced signal for variations introduced by the

diode ***D***, the resulting compensated signal ***E*** is closely proportional to the back EMF voltage ***e***.

[41] **FIG. 7** is a theoretical timing diagram illustrating the compensated signals ***Ea***, ***Eb***, ***Ec*** at the nodes ***Nea***, ***Neb***, and ***Nec*** of precondition circuit ***50*** of **FIG. 6**, and resulting output from the zero-crossing detection circuit ***52*** in a motor, according to an embodiment of the invention. For sake of simplicity, the theoretical data shown in **FIG. 7** presumes the high frequency PWM signal is removed. As shown, with the precondition circuit ***50*** compensating for the offset caused by the diode ***D***, the output of the zero-crossing detection circuit ***52*** that controls advancement of the commutation sequence of the motor is substantially reflects the desired 60-degree switching intervals. Accordingly, an aspect of the present invention provides for smoother switching through the commutation sequence, which in turn provides a more efficient motor that is less likely to jitter or stall.

[42] Although the invention has been shown and described with respect to certain preferred embodiments, it is obvious that equivalents and modifications will occur to others skilled in the art upon the reading and understanding of the specification. Alternatively, while the networks ***50a-c*** of the precondition circuit ***50*** and zero-crossing detection circuits ***52*** are depicted as separate components for each phase, it will be appreciated that such circuitry may be combined into fewer circuits and/or fully consolidated without departing from true spirit or scope of invention. Therefore, embodiments of the present invention include all such equivalents and modifications, and are limited only by the scope of the following claims.